

[0020] As shown in FIG. 2, the system has been repartitioned (at line A-A or B-B of FIG. 1), to move the panel controller closer to the graphics controller. This is especially beneficial in small form factor systems, such as laptop computers, cell phones, palm computers, and the like, in which it is known a priori that the display panel will not be located a long distance from the graphics controller. In some prior art systems, it was felt to be beneficial to use a high-voltage serial cable (38 in FIG. 1) to carry the pixel data, to minimize line losses and reduce noise effects and avoid parallel cross-talk. However, especially (but not exclusively) when the display panel is a short distance from the video engine, a parallel and lower-voltage link 72 can be advantageously employed.

[0021] FIG. 3 illustrates one exemplary embodiment of the link 72 which couples the panel controller and the display panel. The reader will appreciate that other embodiments are very much possible and within the scope of this invention. In the following explanation, the shorthand “wire” will be used to indicate a single communication path or channel, and should not be misunderstood to be limited to e.g. a single strand of copper wire. In the example shown, a synchronizing clock signal CLK is provided over a single wire, a reset signal RESET# is provided over a single wire, a vertical synchronization signal VSYNC# is provided over a single wire, a pair of horizontal synchronization signals HSYNC#[1:0] are provided over two wires, and three color indication signals COLOR#[2:0] are provided over three wires.

[0022] There are also a number of data signals DATA# which carry the pixel data. In various embodiments, this data bus can have various widths. There is no theoretical minimum or maximum width. In the embodiment shown, there are two data signals DATA#[1:0] that also serve as configuration lines, and the remaining data wires, are designated as DATA#[X:2]. The number of configuration lines is not limited to exactly two.

[0023] FIG. 4 illustrates a timing diagram of one exemplary set of such signals during one embodiment of a power-on configuration cycle, in which the display panel provides configuration parameters to the display controller, to configure the generic display controller to work specifically with that display panel.

[0024] There are many characteristics of a display panel for which such configuration may be desirable. The skilled reader will readily appreciate that this invention may be practiced in a wide variety of configurable panel controllers and display panels, and that the various sets of parameters may differ from case to case. Examples of such parameters include but are not limited to:

TABLE 1

Example Parameters	
Resolution	the number of pixels, specified in terms of columns and rows (aka scan lines) in the display panel, typically expressed as a pair of numbers
Data Bus Width	the number of DATA# wires
Display Technology	Cathode Ray Tube (CRT), Liquid Crystal Display (LCD), Organic Light-Emitting Diode (OLED) display, or the like

TABLE 1-continued

Example Parameters	
Gray Scale Support	how many levels of contrast the panel supports in monochrome mode
Modulation Index	the number of bits/pin/clock
Scan Type	progressive or interlaced
Color Space	RGB, YUV, etc.
Min Clock Frequency	lowest clock rate that the display can accept
Max Clock Frequency	highest clock rate that the display can accept
Preferred Clock	the display's preferred clock rate
Scan Rate	frame rate or vertical refresh frequency
Degradation	intensity or color adjustment needed to compensate for aging of display
Color Depth	how many bits of color are supported by the panel's DACs

[0025] In order that the panel controller be able to communicate with a large variety of panels, it is desirable that the configuration information be transferred to the panel controller over wire(s) that are present in the largest quantity of potential panels. In one mode, the low-order two bits DATA#[1:0] of the pixel data wires are used to carry the configuration parameters to the panel controller, as shown in FIG. 4. The reader may also wish to make continued reference also to FIG. 2.

[0026] At some arbitrary time, the panel controller takes the RESET# signal active (low) then inactive, resetting the power-on configuration logic, which runs through its POST (typically in clock cycles that are shown in FIG. 4 as a single cycle 0 for ease of illustration). In synchronism with the CLK signal, with VSYNC# active and HSYNC#[1] inactive, the machine is in a configuration cycle. HSYNC#[0] is a don't care, in this embodiment of the invention.

[0027] At either a predetermined or an arbitrary number of clock cycles after VSYNC# going active and HSYNC#[1] going inactive, the display panel's power-on control logic (or other suitable means) sends one or more configuration parameters back to the panel controller over the predesignated configuration path, such as DATA#[1:0]. In some embodiments, the actual values of the parameters are passed, such as the numbers 640 and 480 during the Resolution parameter's transfer cycles. In other embodiments, predetermined designators, such as lookup table indices, state machine state numbers, or the like may be passed. Other parameter passing schemes are within the scope of this invention, as well. In some embodiments, parameters may be passed from the controller to the display, in addition to or in lieu of parameters passed from the display to the controller.

[0028] In one embodiment, the Resolution is passed over four clock cycles, the Data Bus Width (“Width”) is passed over four clock cycles, the Display Technology (“Disp.”) is passed over two clock cycles, the Gray Scale Support (“GS”) is passed over two clock cycles, the Modulation Index (“MI”) is passed over two clock cycles, and the Scan Type (“PI”) is passed over one clock cycle. Other sets of parameters, other orderings, and other numbers of clock cycles are, of course, within the teachings of this patent.

[0029] FIGS. 5 and 6 illustrate more detail concerning the Modulation Index functionality. Double-pumped and quad-pumped busses are known, such as those of the Intel@